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Application Note 1145

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A Compendium of Application Circuits for Intersil Digitally-Controlled (XDCP) Potentiometers

Introduction

This application note lists a number of application circuits for Intersil's digitally-controlled (XDCP) potentiometers. The application circuits illustrate the wide variety of possible functions which can be implemented using the variability of the potentiometer in conjunction with standard active devices like operational amplifiers and comparators. The types of circuits include control circuits, converters, filters, signal processing circuits, regulators, wave shapers, analog computing circuits and signal sources. The circuits are shown in basic form and do not include supply decoupling or proper grounding techniques. The user must account for these in the final design.

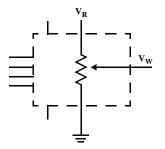
Intersil's potentiometers are controlled through the 2-wire, I²C, 3-wire, or SPI computer serial-interfaces or buses. For front panel, push button type applications, Intersil's push pots are recommended.

Electronic digitally-controlled (XDCP) potentiometers provide three powerful application advantages:

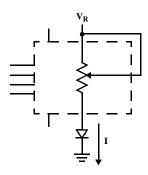
- 1. The variability and reliability of a solid-state potentiometer.
- 2. The flexibility of computer-based digital controls.
- 3. The retentivity of nonvolatile memory used for the storage of multiple potentiometer settings or data.

In addition, the packages of the potentiometers are completely compatible with other electronic components and hence reduce manufacturing assembly costs.

Applications



THREE TERMINAL POTENTIOMETER; VARIABLE VOLTAGE DIVIDER



TWO TERMINAL VARIABLE RESISTOR; VARIABLE CURRENT

FIGURE 1. BASIC CONFIGURATIONS OF ELECTRONIC POTENTIOMETERS

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Application Circuits

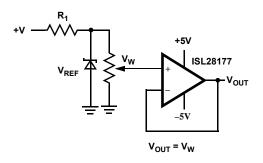
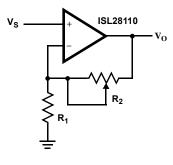


FIGURE 2. BUFFERED REFERENCE VOLTAGE



 $V_0 = (1+R_2/R_1)V_S$

FIGURE 4. NONINVERTING AMPLIFIER

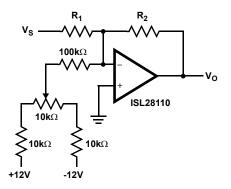


FIGURE 6. OFFSET VOLTAGE ADJUSTMENT

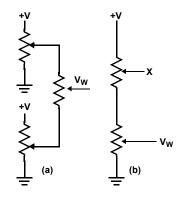
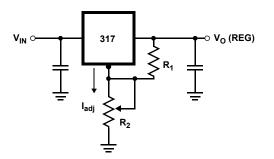


FIGURE 3. CASCADING TECHNIQUES



 V_{O} (REG) = 1.25V (1+R₂/R₁)+I_{adj} R₂

FIGURE 5. VOLTAGE REGULATOR

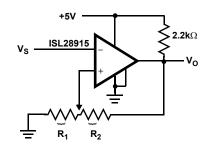
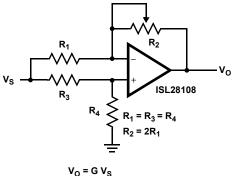


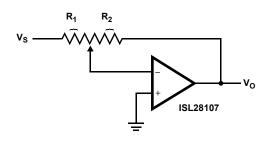
FIGURE 7. COMPARATOR WITH HYSTERISIS

Application Circuits (Continued)



V_O = G V_S -1/2 ≤ G ≤ +1/2

FIGURE 8. ATTENUATOR



 $V_0 = G V_S$ $G = - R_2/R_1$

FIGURE 10. INVERTING AMPLIFIER

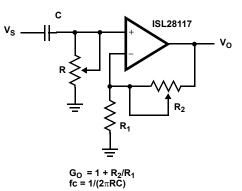
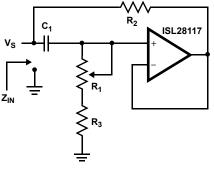
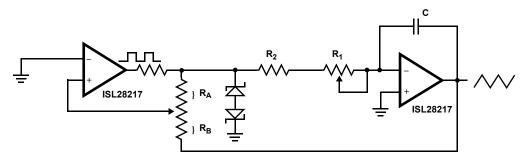


FIGURE 9. FILTER



 $Z_{IN} = R_2 + s R_2 (R_1 + R_3) C_1 = R_2 + s Leq$ (R₁ + R₃) >> R₂

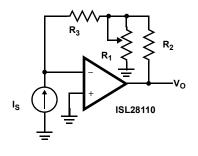
FIGURE 11. EQUIVALENT L-R CIRCUIT

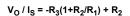


 $\begin{array}{l} \text{FREQUENCY} \propto R_1,\,R_2,\,\text{C} \\ \text{AMPLITUDE} \propto R_A,\,R_B \end{array}$

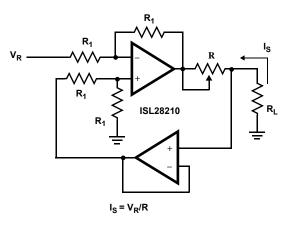
FIGURE 12. FUNCTION GENERATOR

Application Circuits (Continued)

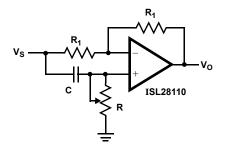






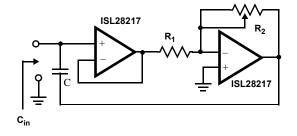






 \angle V₀/V_S = 180° – 2tan⁻¹ ω RC





 $C_{IN} = C (1 + R_2/R_1)$



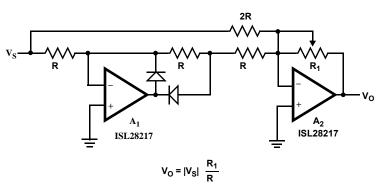
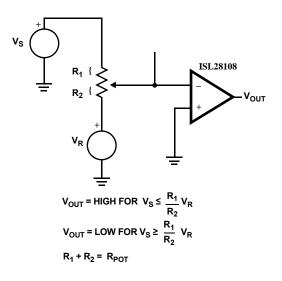
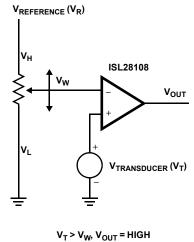


FIGURE 17. ABSOLUTE VALUE AMPLIFIER WITH GAIN

Application Circuits (Continued)

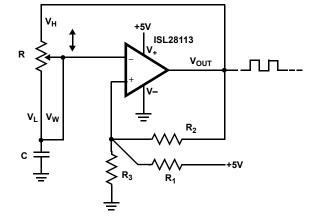




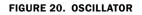
 $V_T < V_W, V_{OUT} = LOW$

FIGURE 18. LEVEL DETECTOR





Frequency \propto R, C Duty Cycle \propto R₁, R₂, R₃



+5V

С

ISL28113

VOUT

Application Circuits (Continued)

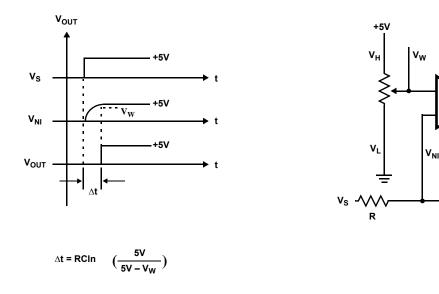


FIGURE 21. TIME DELAY

Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that the Application Note or Technical Brief is current before proceeding.

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